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PATENT
(5181-68300/P5074)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/755,479
Filed: January 4, 2001
Inventor(s):
Whay S. Lee

Title: A Scalable Routing Scheme for a Multi-Path Interconnection Fabric

Examiner: Unknown
Group/Art Unit: 2151
Atty. Dkt. No: 5181-68300

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Robert C. Kowert
Name of Registered Representative

Signature

August 22, 2001
Date

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☒ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☒ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

U.S. Patent Application Serial No. 09/850,930 (5181-75500)
U.S. Patent Application Serial No. 09/851,299 (5181-75400)
U.S. Patent Application Serial No. 09/740,132 (5181-68600)
U.S. Patent Application Serial No. 09/740,130 (5181-73000)
U.S. Patent Application Serial No. 09/739,924 (5181-75300)

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

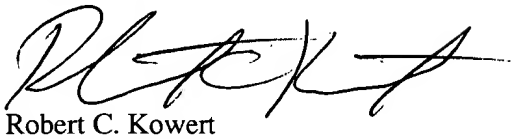
6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5181-68300/RCK.

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
Attorney for Applicant(s)

CONLEY, ROSE & TAYON, P.C.
P. O. Box 398
Austin, Texas 78767
(512) 476-1400

Date: August 22, 2001

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5181-68300 APPLICANT: Lee FILING DATE: January 4, 2001	SERIAL NO. 09/755,479 GROUP: 2151

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	6,016,510	1/18/00	Quattromani, et al.			
	A2	6,023,753	2/8/00	Pechanek, et al.			
	A3	5,689,661	11/18/97	Hayashi, et al.			
	A4	6,167,502	12/26/00	Pechanek, et al.			
	A5	6,101,181	8/8/00	Passint, et al.			
	A6	5,720,025	2/17/98	Wilkes, et al.			
	A7	5,970,232	10/19/99	Passint, et al.			
	A8	6,055,618	4/25/00	Thorson			
	A9	5,701,416	12/23/97	Thorson, et al.			
	A10	5,737,628	4/7/98	Birrittella, et al.			
	A11	5,689,646	11/18/97	Thorson			

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	A12	99/26429	5/27/99	WO			
	A13	0 785 512	7/23/97	EP			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A14	Bradley Kuszmaul, Mercury Computer Systems, Inc., "The RACE Network Architecture," (posted at www.mc.com/techlit/#tech_brief prior to this), 6 pages.
	A15	R.Y. Wang, T.E. Anderson and D.A. Patterson, "Virtual Log Based File Systems For a Programmable Disk," Proc. Third Symposium on Operating Systems Design and Implementation, February 1999 (Also appeared as University of California Technical Report CSD-98-1031, 16 pages.
	A16	Prasant Mohapatra, "Wormhole Routing Techniques for Directly Connected Multicomputer Systems, ACM Computing Surveys, Vol. 30, No. 3, September 1998, 37 pages.
	A17	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Journal of the Association for Computing Machinery, Vol. 41, No. 5, September 1994, pp. 874-902.

EXAMINER: DATE CONSIDERED:

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A18	Reddy, Dept. of Computer & Information Sciences, "A Dynamically Reconfigurable WDM LAN Based on Reconfigurable Circulant Graph," IEEE, 1996, 4 pages.
	A19	Various Abstracts beginning with Funahashi, Jouraku and Amano, "Adaptive Routing for Recursive Diagonal Torus," Transactions of the Institute of Electronics, Information and Communication Engineers D-I, vol. J83D-I, no. 11, November 2000, pp. 1143-53.
	A20	Milan Kovacevic, Center for Telecommunications Research, "On Torus Topologies with Random Extra Links," IEEE 1996, pp. 410-418.
	A21	Dally, et al., The Torus Routing Chip, Distributed Computing, Springer-Verlag 1986, pp. 187-196.
	A22	Susan Hinrichs, "A Compile Time Model for Composing Parallel Programs," IEEE Parallel and Distributed Technology, 1995, 19 pages.
	A23	"CRAY T3D System Architecture Overview Manual," ftp://ftp.cray.com/product-info/mpp/T3D_Architecture_Over/T3D.overview.html, Cray Research, 1993, 40 pages.
	A24	Marco Fillo, et al., "The M-Machine Multicomputer," Laboratory for Computer Science, Massachusetts Institute of Technology, A.I. Memo No. 1532, Ann Arbor,. March 1995, 14 pages.
	A25	Noakes, et al., "The J-Machine Multicomputer: An Architectural Evaluation," Proceedings of the 20th International Symposium on Computer Architecture, May 1993, 12 pages.
	A26	Dally, et al., "Architecture of a Message-Driven Processor," International Conference on Computer Architecture, June 1987, pp. 189-196.
	A27	Dennison, Lee and Dally, "High-Performance Bidirectional Signalling in VLSI," Massachusetts Institute of Technology, October 12, 1992, 20 pages.
	A28	Dally, et al., "Architecture and Implementation of the Reliable Router," Mass. Institute of Technology, Proceedings of Hot Interconnects II, Stanford CA, August 1994, 12 pages.
	A29	Dally, et al., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers," Proceedings of the First International Parallel Computer Routing and Communication Workshop, Seattle WA, May 1994, 15 pages.
	A30	Dennison, et al., "Low-Latency Plesiochronous Data Retiming," Mass. Institute of Technology, Proceedings of the 1995 Advanced Research in VLSI Conference, Chapel Hill NC, March 1995, 12 pages
	A31	Whay S. Lee, "Mechanism for Efficient, Protected Messaging," Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, January 20, 1999, 147 pages.
	A32	Dennison, "Reliable Interconnect Networks for Parallel Computers," Mass. Institute of Technology, Dept. of Electrical Engineering and Computer Science, April 18, 1991, 79 pages.
	A33	Thucydides Xanthopoulos, "Fault Tolerant Adaptive Routing in Multicomputer Networks," Dept. of Electrical Engineering and Computer Science , Mass. Institute of Technology, January 20, 1995, 152 pages.
	A34	Dennison, "The Reliable Router: An Architecture for Fault Tolerant Interconnect," Dept. of Electrical Engineering and Computer Science, Mass Institute of Technology, May 24, 1996, 145 pages.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A35	"Introduction To Parallel Algorithms and Architectures: Arrays, Trees, Hypercubes," F. Thomson Leighton, Morgan Kaufmann Publishers, 1992, pp. 1-831.
	A36	Christopher J. Glass and Lionel Ni, "Fault-Tolerant Wormhole Routing in Meshes," Technical Report, MSU-CPS-ACS-72, October 30, 1992 (revised May 25, 1993), 28 pages.
	A37	Stefan Savage and John Wilkes, "AFRAID-A Frequently Redundant Array of Independent Disks," Proceedings of the 1996 USENIX Technical Conference, pp. 27-39, San Diego, CA, January 1996, 13 pages.
	A38	Steve Ward, et al., "A Modular, Scalable Communications Substrate," MIT Laboratory for Computer Science, July 1993, 10 pages.
	A39	Christopher Glass and Lionel Ni, "The Turn Model for Adaptive Routing," Technical Reports, MSU-CPS-ACS-44, October 10, 1991 (revised March 2, 1992), pages 278-287 (numbered herein as 1-20).
	A40	Thomas Stricker, "Message Routing on Irregular 2D-Meshes and Tori," School of Computer Science, Carnegie Mellon Univ., January 15, 1991, pages 170-177 (numbered herein as 1-19).
	A41	Dally, et al., "The J-Machine: A Restrospective," in 25 Years of the International Symposia on Computer Architecture - Selected Papers. Pp. 54-58

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